

1. A method for dynamic adjustment of priority and step procedures for determining effective lot dispatching for wafer and chip probing, comprising:
  - a. using two-phased, event-driven dispatching system structure for said dynamic adjustment;
  - b. using said step procedures to choose lots that can utilize incorporated auxiliary apparatus without need for new setup;
  - c. providing for engineering lots capacity check in said step procedures;
  - d. solving dispatching conflict between wafer and package lots, and
  - e. limiting tester's capability in product through use of common constraint system.
2. The method for dynamic adjustment of priority and step procedures of claim 1, wherein said two-phased, event-driven dispatching system structure to comprises of lot rank and lot assignment.
3. The method for dynamic adjustment of priority and step procedures of claim 2, wherein said lot rank to comprises of a lot rank priority formula for production wafers and packages and a lot rank for engineering lots.
4. The method for dynamic adjustment of priority and step procedures of claim 3, wherein said priority formula of: Priority =  $\sum (Base * Weight_x)$  calculates priority.

5. The method for dynamic adjustment of priority and step procedures of claim 2, wherein said lot assignment to comprises of exception lots, hot run, super hot run, normal lot, and engineering lot dispatching rule with the object of being based on Master Production Schedule target to reduce setup time.
6. The method for dynamic adjustment of priority and step procedures of claim 1, wherein dispatch in a test foundry can be affected by performance indices, special dispatch properties, auxiliary apparatus, tester constraints, and production mode.
7. The method for dynamic adjustment of priority and step procedures of claim 1, wherein said auxiliary apparatus includes tester, probe card, and load board.
8. The method for dynamic adjustment of priority and step procedures of claim 1, wherein a multi-priority factor and multi-dispatching step procedure is enhanced to fit complex dispatching demands of a test foundry and used with different operation types such as chip probing and final testing.
9. The method for dynamic adjustment of priority and step procedures of claim 1, wherein said method is based on distinct production goals or behavior reported by production and engineering devices to in real time get the most desirable dispatching list for a particular

tester at any given time.

10. The method for dynamic adjustment of priority and step procedures of claim 1, wherein said step procedures are expanded to consider different product lots in addition to same products to said utilize any same said auxiliary apparatus without need for new set up.
11. The method for dynamic adjustment of priority and step procedures of claim 1, wherein said engineering lot capacity limitation check is done to see if the amount of fixed testing time per week determined by testing site personnel for engineering lots to be tested on any particular machine has been exceeded.
12. The method for dynamic adjustment of priority and step procedures of claim 11, wherein said engineering lots are dispatched automatically with manual effort only needed for setting exception rules and taking care of special cases thereby eliminating need for manual dispatching sheet.
13. The method for dynamic adjustment of priority and step procedures of claim 1, wherein said dispatching conflict between wafer and package lots is avoided by having said step procedures make sure no wafer work in progress remains before allowing said package lots to be dispatched with the result of minimal changeovers.

14. The method for dynamic adjustment of priority and step procedures of claim 13, wherein said package lots are treated as an engineering step procedure with added considerations of dispatching a same product or same production type as a lot just tested and resource constraint of a load board.
15. The method for dynamic adjustment of priority and step procedures of claim 1, wherein said common constraint system is a PROMIS constraint system.
16. The method for dynamic adjustment of priority and step procedures of claim 15, wherein said PROMIS constraint system provides a function for users to limit said tester's product capability from which said step procedure's last step is to check said PROMIS constraint system to filter out inappropriate lots to avoid mistake operations.
17. A system for dynamic adjustment of priority and step procedures for determining effective lot dispatching for wafer and chip probing, comprising:
  - a. a means to use a two-phased, event-driven dispatching system structure for said dynamic adjustment;
  - b. a means to use said step procedures to choose lots that can utilize incorporated auxiliary apparatus without need for new setup;
  - c. a means to provide engineering lots capacity check in said step procedures;
  - d. a means to solve dispatching conflict between wafer and package lots, and

- e. means to limit tester's capability in product through constraint.
18. The system for dynamic adjustment of priority and step procedures of claim 17, wherein said two-phased, event-driven dispatching system structure to comprises of lot rank and lot assignment.
19. The system for dynamic adjustment of priority and step procedures of claim 18, wherein said lot rank to comprises of a lot rank priority formula for production wafers and packages and a lot rank for engineering lots.
20. The system for dynamic adjustment of priority and step procedures of claim 19, wherein said priority formula of: Priority =  $\sum (Base * Weight)$  calculates priority.
21. The system for dynamic adjustment of priority and step procedures of claim 18, wherein said lot assignment to comprises of exception lots, hot run, super hot run, normal lot, and engineering lot dispatching rule with the object of being based on Master Production Schedule target to reduce setup time.
22. The system for dynamic adjustment of priority and step procedures of claim 17, wherein dispatch in a test foundry can be affected by performance indices, special dispatch

properties, auxiliary apparatus, tester constraints, and production mode.

23. The system for dynamic adjustment of priority and step procedures of claim 17, wherein said auxiliary apparatus includes tester, probe card, and load board.
24. The system for dynamic adjustment of priority and step procedures of claim 17, wherein a multi-priority factor and multi-dispatching step procedure is enhanced to fit complex dispatching demands of a test foundry and used with different operation types such as chip probing and final testing.
25. The system for dynamic adjustment of priority and step procedures of claim 17, wherein based on distinct production goals or behavior reported by production and engineering devices to in real time get the most desirable dispatching list for a particular tester at any given time.
26. The system for dynamic adjustment of priority and step procedures of claim 17, wherein said step procedures are expanded to consider different product lots in addition to same products to said utilize any same said auxiliary apparatus without need for new set up.
27. The system for dynamic adjustment of priority and step procedures of claim 17, wherein said engineering lot capacity limitation check is done to see if the amount of fixed testing

time per week determined by testing site personnel for engineering lots to be tested on any particular machine has been exceeded.

28. The system for dynamic adjustment of priority and step procedures of claim 27, wherein said engineering lots are dispatched automatically with manual effort only needed for setting exception rules and taking care of special cases thereby eliminating need for manual dispatching sheet.
29. The system for dynamic adjustment of priority and step procedures of claim 17, wherein said dispatching conflict between wafer and package lots is avoided by having said step procedures make sure no wafer work in progress remains before allowing said package lots to be dispatched with the result of minimal changeovers.
30. The system for dynamic adjustment of priority and step procedures of claim 29, wherein said package lots are treated as an engineering step procedure with the added considerations of dispatching the same product or same production type as the lot just tested and resource constraint of said load board.
31. The system for dynamic adjustment of priority and step procedures of claim 17, wherein said common constraint system is the PROMIS constraint system.

**TS01-1457**

32. The system for dynamic adjustment of priority and step procedures of claim 31, wherein said PROMIS constraint system provides a function for users to limit said tester's product capability from which said step procedure's last step is to check said PROMIS constraint system to filter out inappropriate lots to avoid mistake operations.